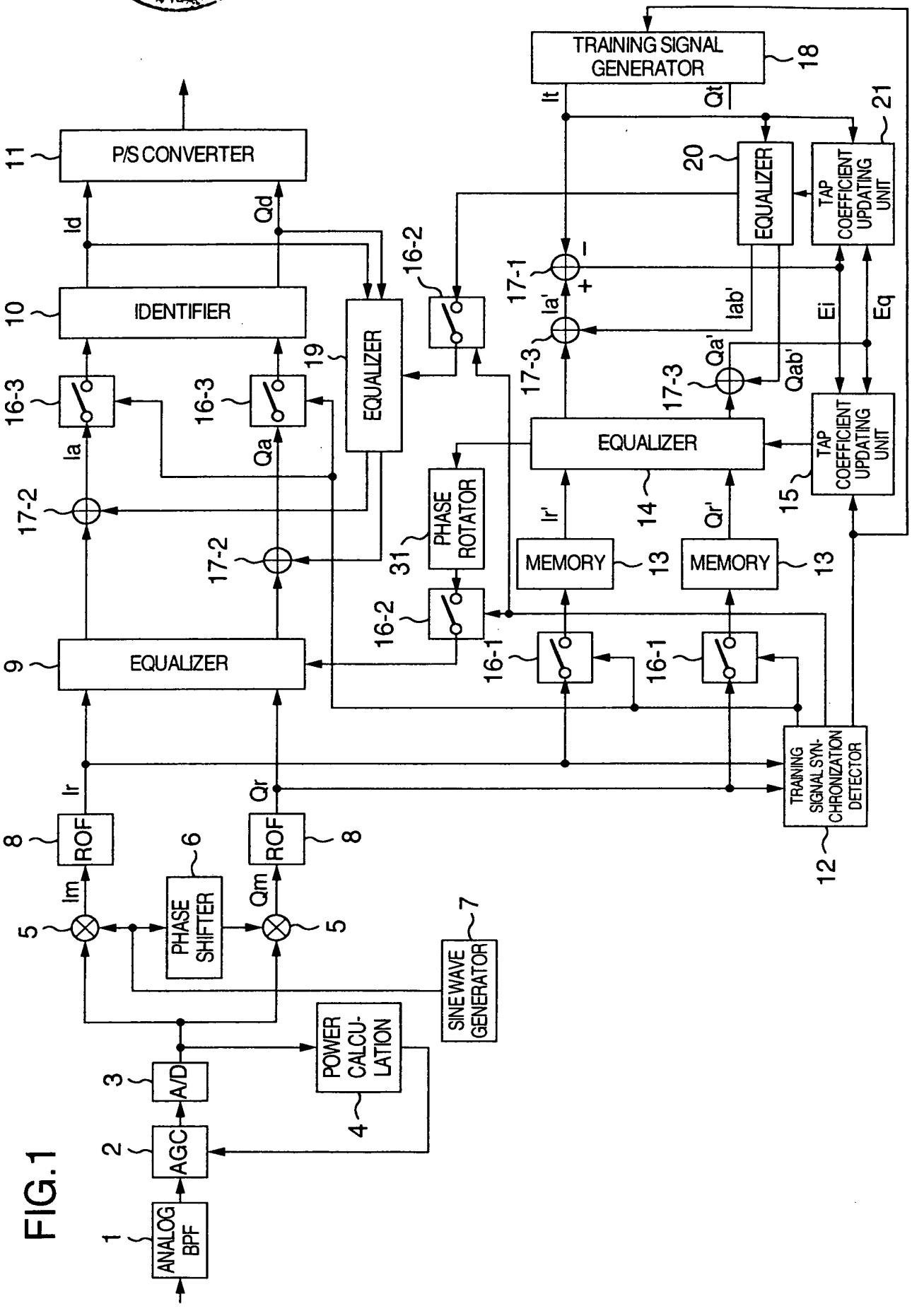



FIG.1

FIG.2

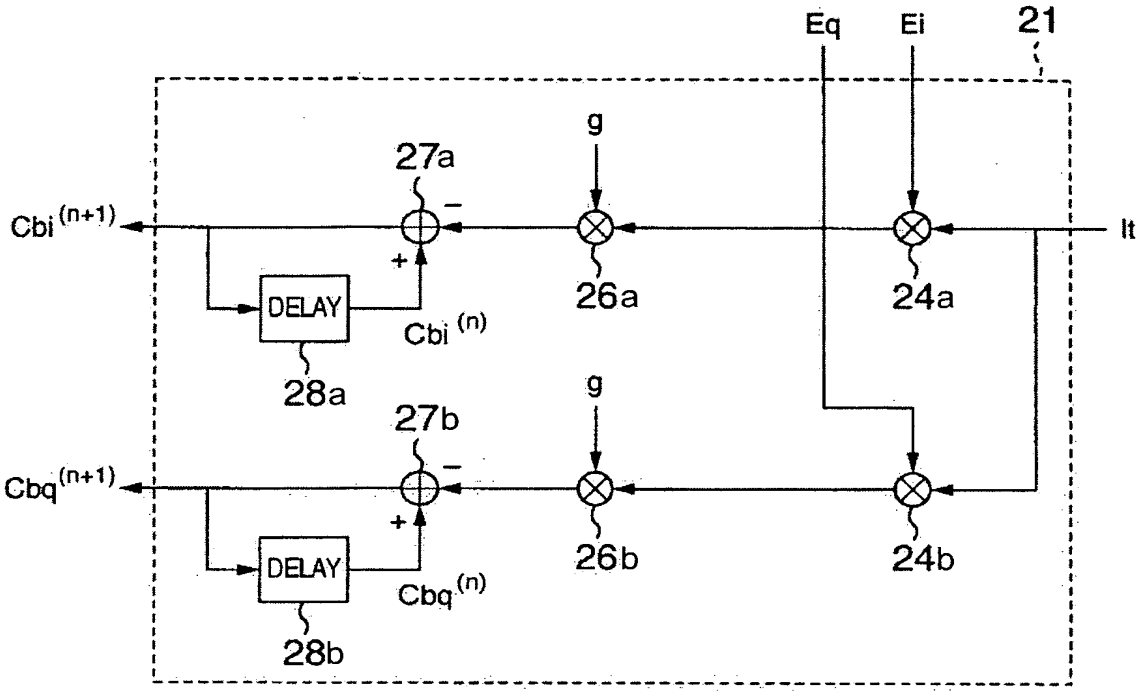

Eq
Ei
21
g
27a
Cbi (n+1)
It
DELAY
Cbi (n)
26a
24a
28a
27b
g
Cbq (n+1)
DELAY
Cbq (n)
26b
24b
28b

FIG.3

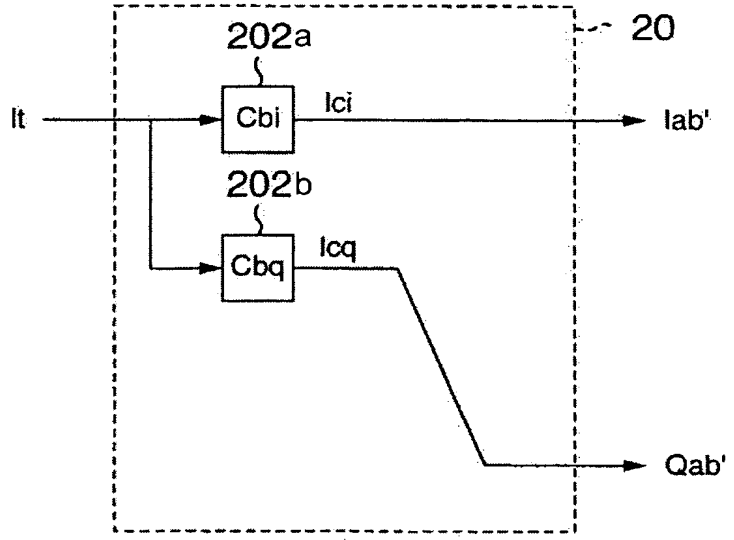

20
202a
It
Cbi
Ici
Iab'
202b
Cbq
Icq
Qab'

FIG.4

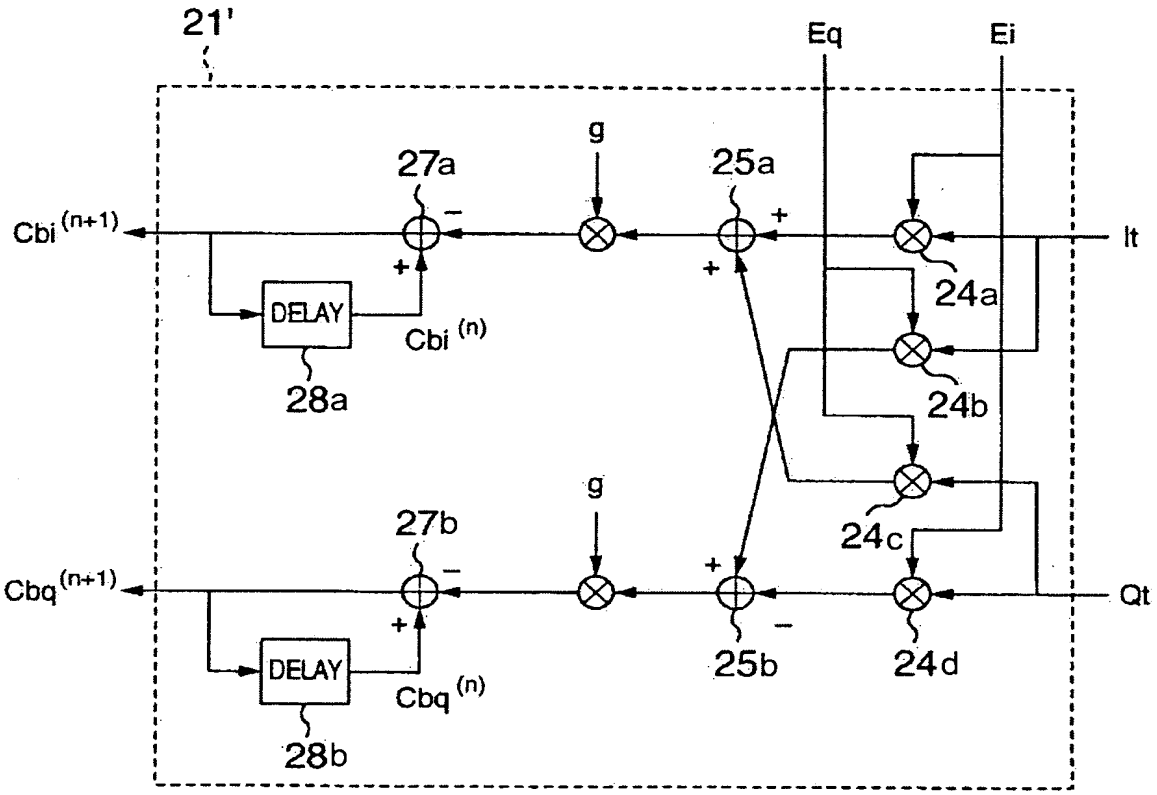

21'
Eq
Ei
g
27a
25a
Cbi (n+1)
It
DELAY
Cbi (n)
28a
24a
24b
24c
27b
Cbq (n+1)
Qt
DELAY
Cbq (n)
28b
25b
24d

FIG.5

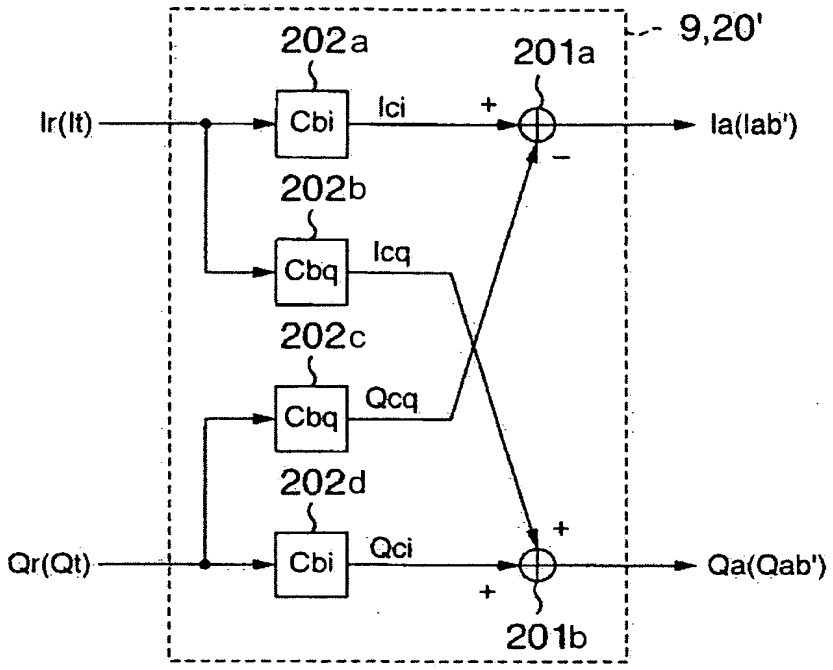

9,20'
202a
201a
Ir(It)
Cbi
Ici
+
Ia(Iab')
−
202b
Cbq
Icq
202c
Cbq
Qcq
202d
Qr(Qt)
Cbi
Qci
+
+
Qa(Qab')
201b

FIG.6

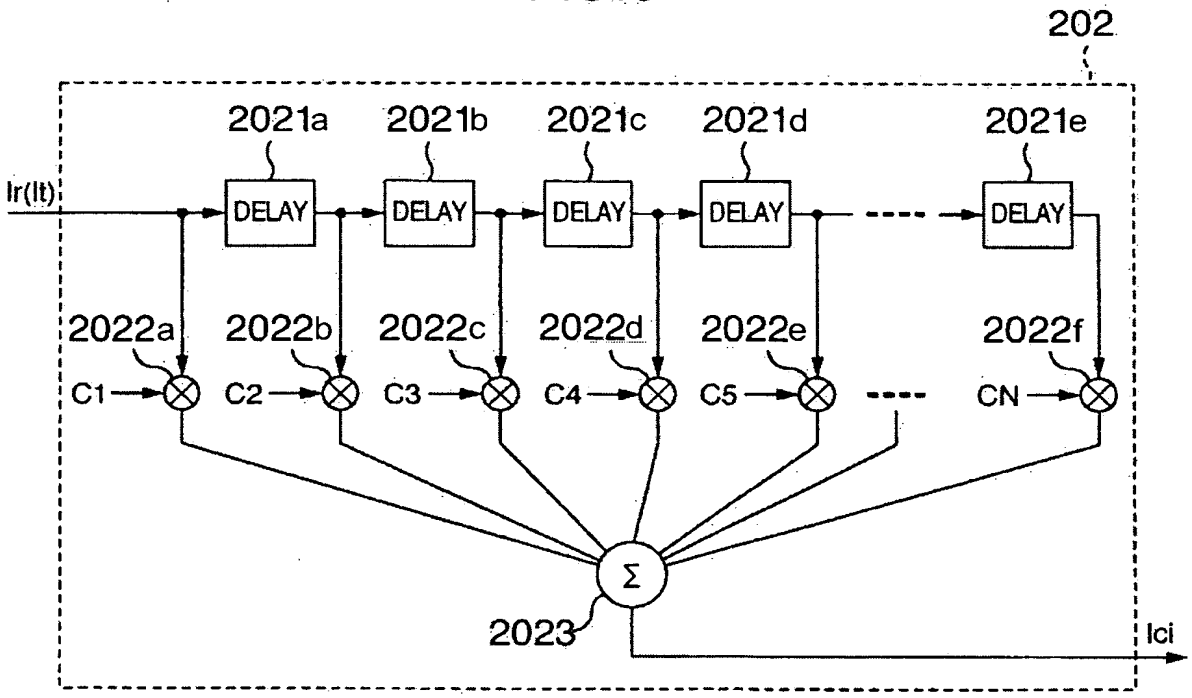

202
2021a
2021b
2021c
2021d
2021e
Ir(It)
DELAY
DELAY
DELAY
DELAY
DELAY
2022a
2022b
2022c
2022d
2022e
2022f
C1
C2
C3
C4
C5
CN
Σ
2023
Ici

FIG.7

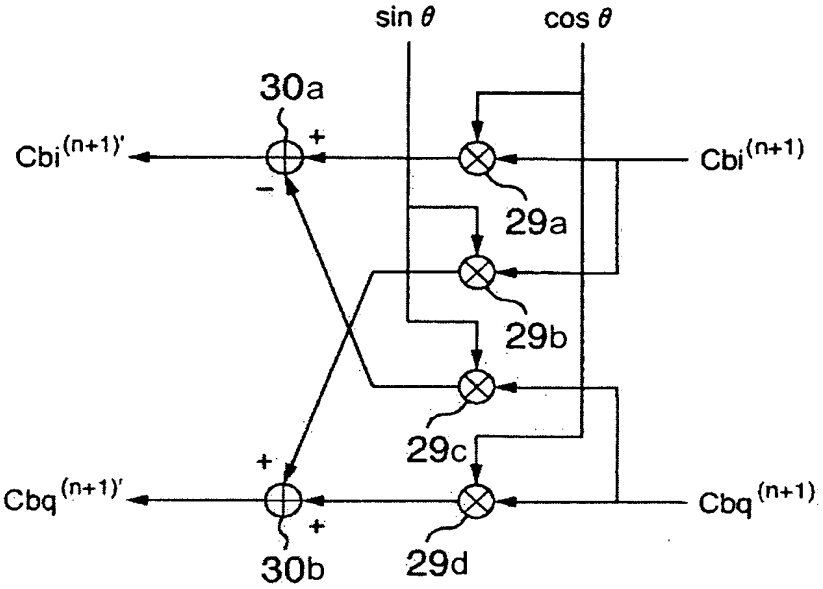
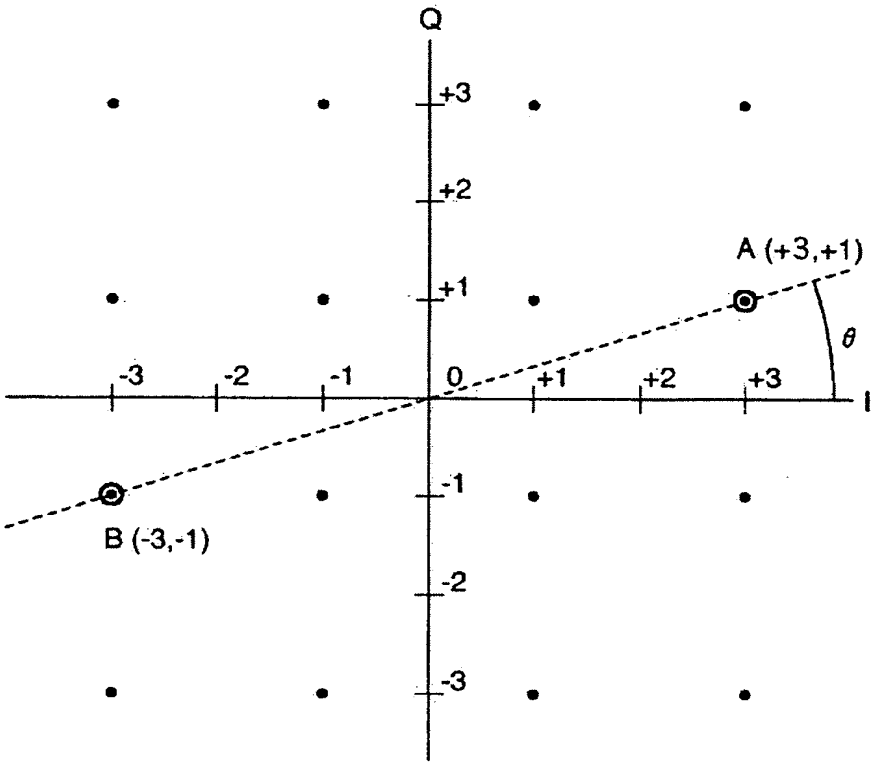
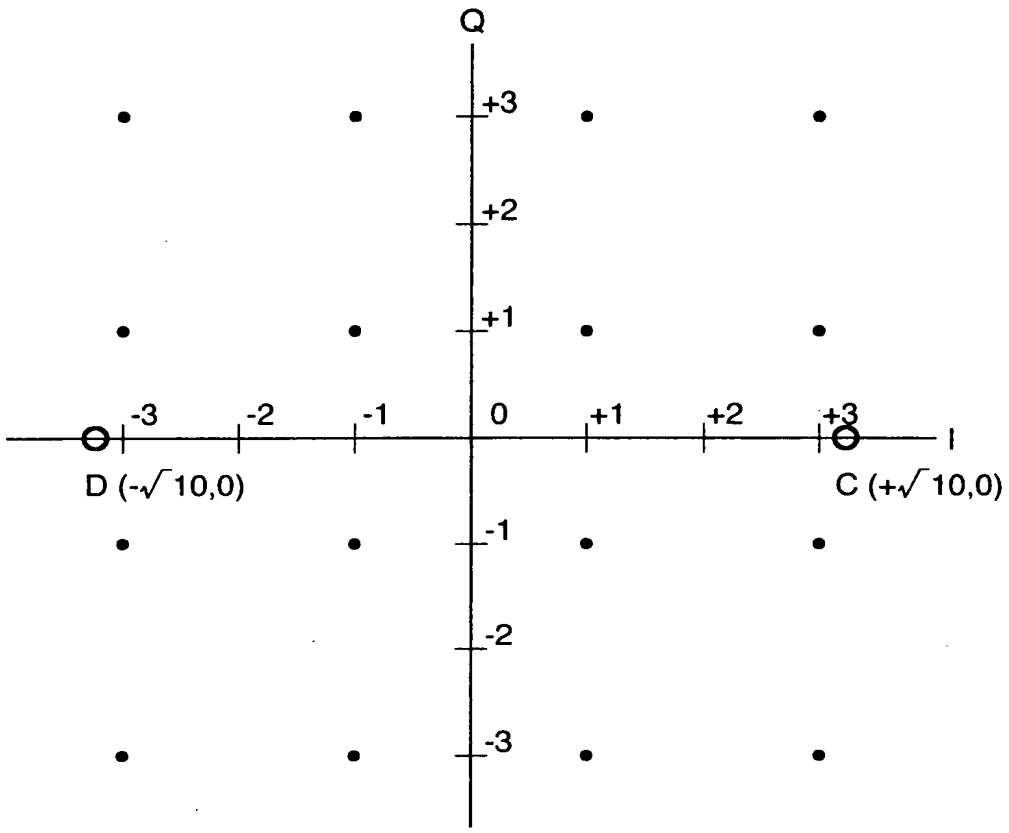



FIG.8




◎ SIGNAL POINT OF TRAINING SIGNAL

FIG.9




O SIGNAL POINT OF TRAINING SIGNAL

FIG.10

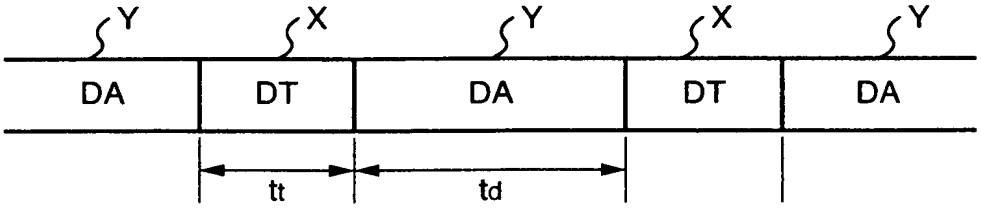
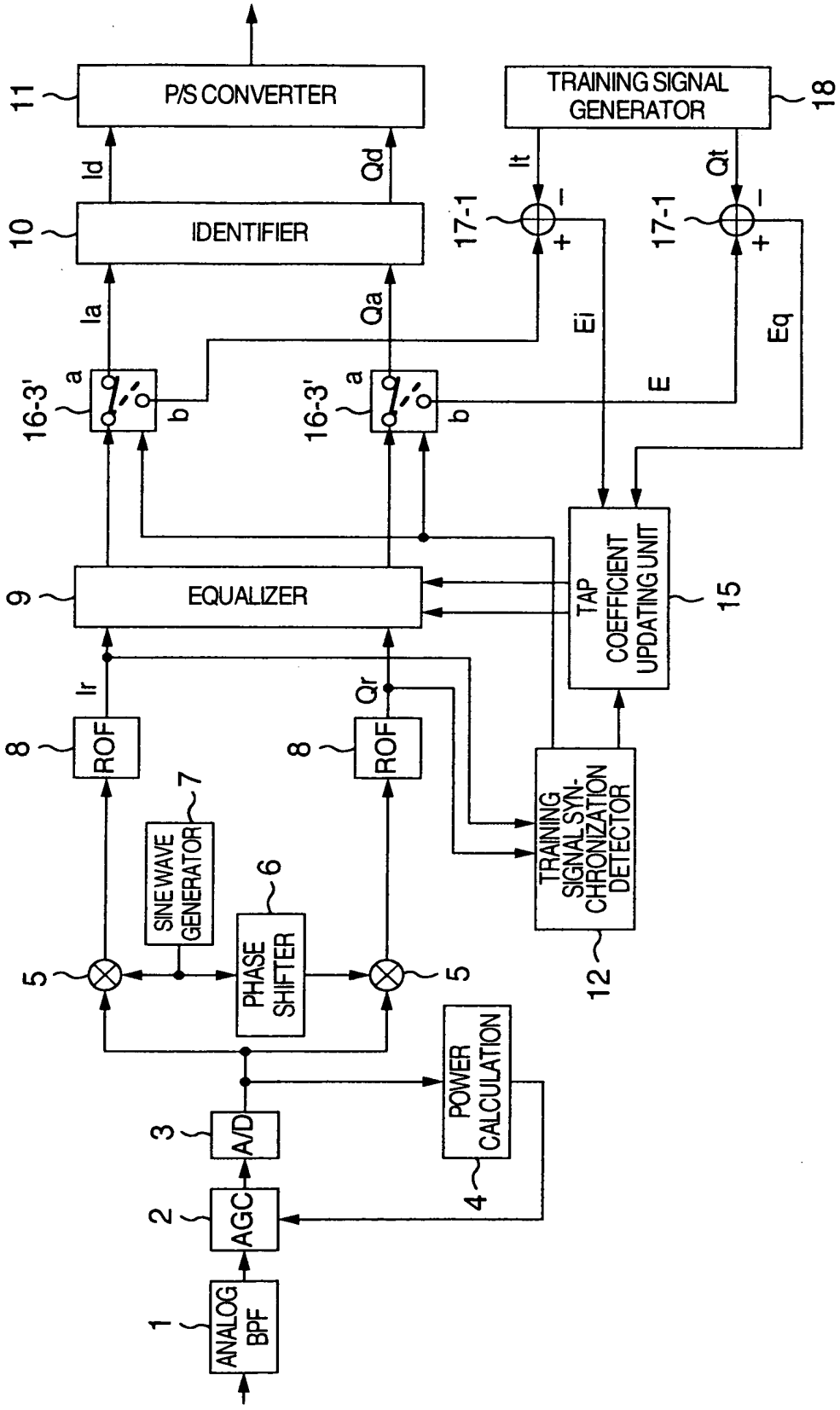


FIG.11
PRIOR ART



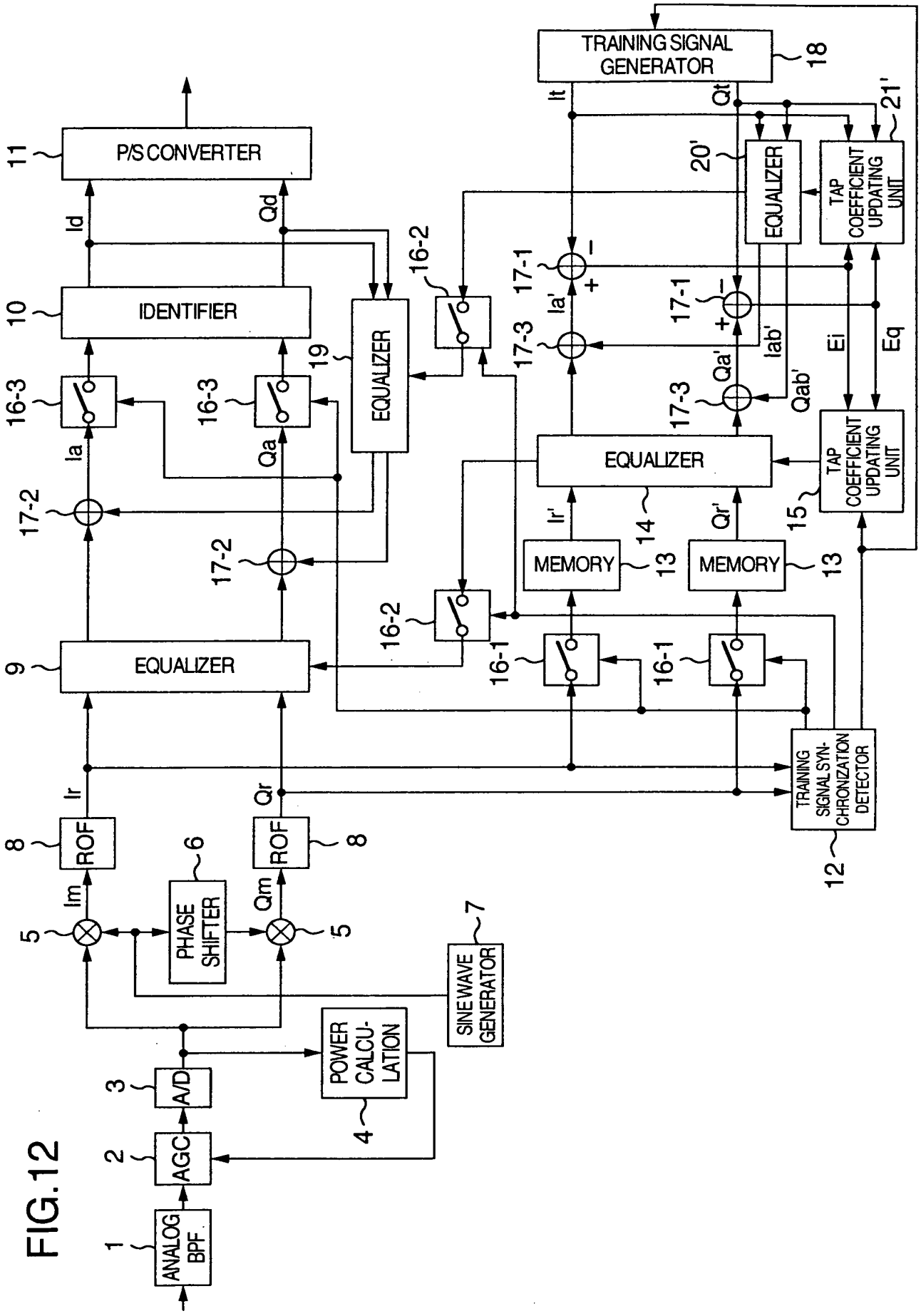

ANALOG BPF
1
AGC
2
A/D
3
POWER CALCU-LATION
4
SINE WAVE GENERATOR
7
PHASE SHIFTER
6
ROF
8
ROF
8
Im
Qm
5
5
Ir
Qr
EQUALIZER
9
IDENTIFIER
10
P/S CONVERTER
11
Id
Qd
16-3
16-3
Ia
Qa
17-2
17-2
EQUALIZER
19
16-2
16-2
16-1
16-1
MEMORY
13
MEMORY
13
Ir'
Qr'
EQUALIZER
14
TAP COEFFICIENT UPDATING UNIT
15
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
12
TRAINING SIGNAL GENERATOR
18
It
Qt
21'
20'
EQUALIZER
TAP COEFFICIENT UPDATING UNIT
17-1
17-1
17-3
17-3
Ia'
Qa'
Iab'
Qab'
Ei
Eq

FIG.12

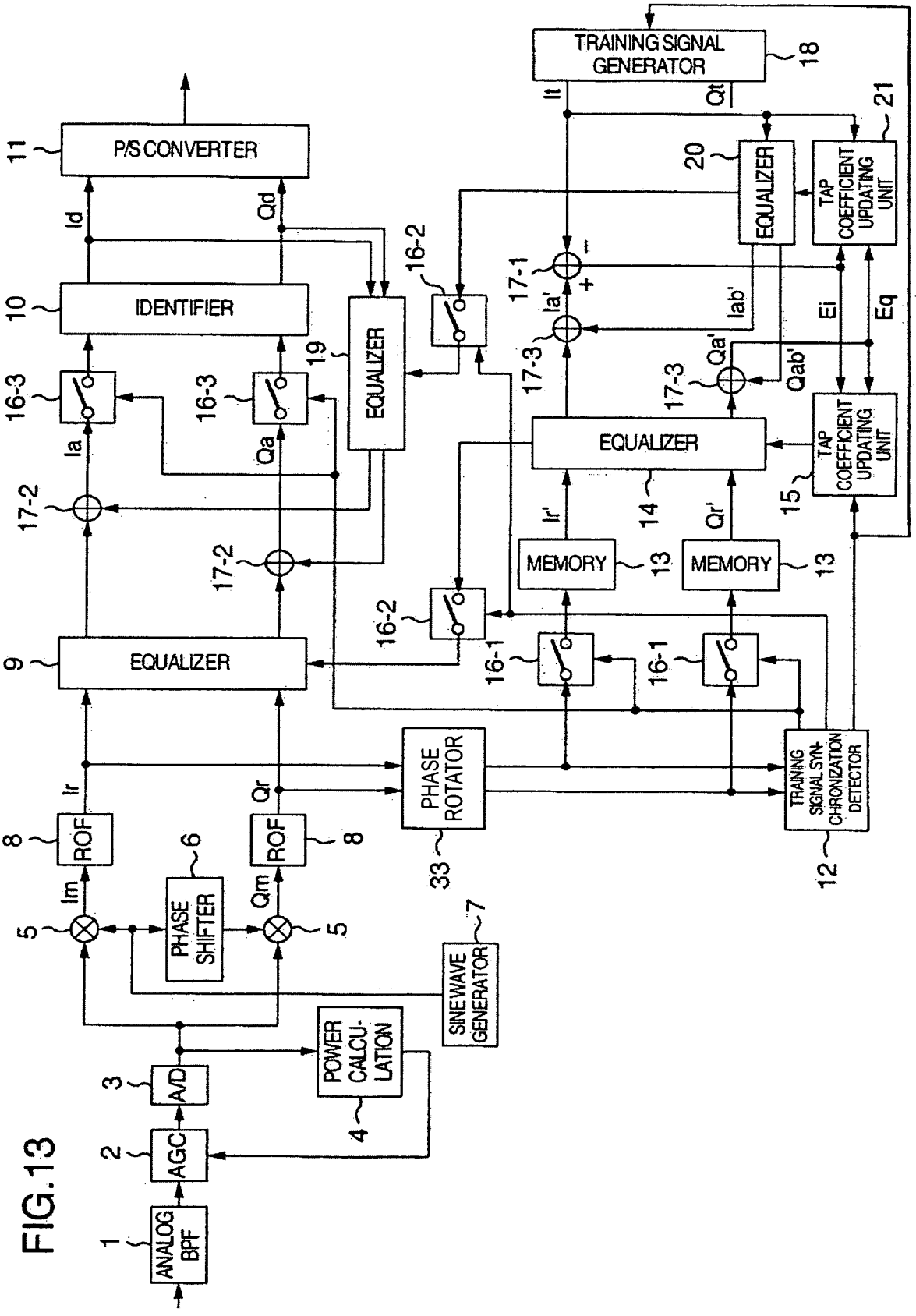

ANALOG BPF
1
AGC
2
A/D
3
POWER CALCU-LATION
4
SINEWAVE GENERATOR
7
PHASE SHIFTER
6
5
5
ROF
8
ROF
8
Im
Qm
Ir
Qr
PHASE ROTATOR
33
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
12
EQUALIZER
9
EQUALIZER
19
16-1
16-1
16-2
16-2
16-3
16-3
17-2
17-2
Ia
Qa
MEMORY
13
MEMORY
13
Ir'
Qr'
14
EQUALIZER
15
TAP COEFFICIENT UPDATING UNIT
17-3
17-3
Qa'
Qab'
Ei
Eq
17-1
Ia'
Iab'
EQUALIZER
20
TAP COEFFICIENT UPDATING UNIT
21
TRAINING SIGNAL GENERATOR
18
It
Qt
IDENTIFIER
10
P/S CONVERTER
11
Id
Qd

FIG.13

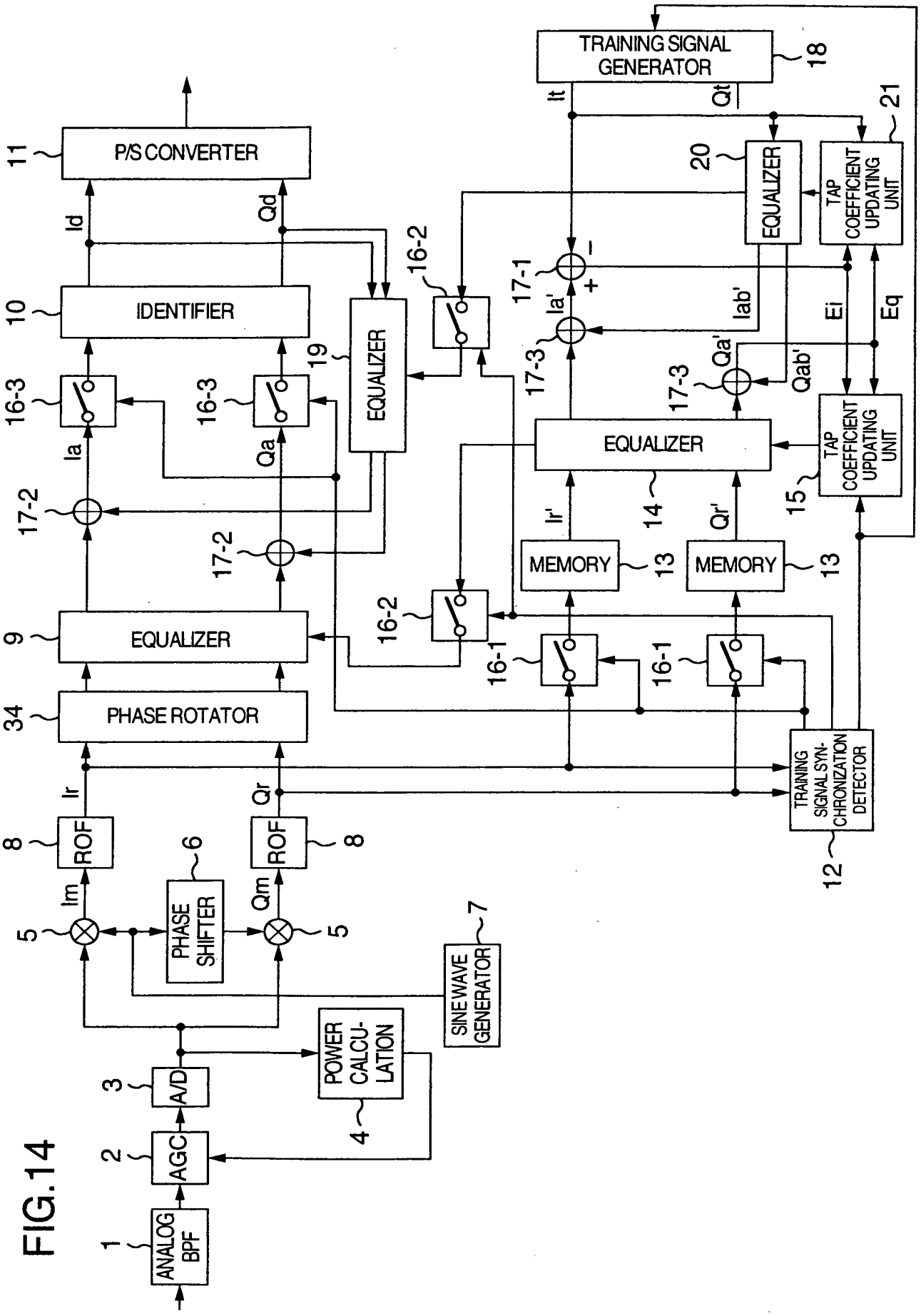

ANALOG BPF
1
AGC
2
A/D
3
POWER CALCU-LATION
4
SINE WAVE GENERATOR
7
PHASE SHIFTER
6
5
Im
Qm
ROF
8
Ir
Qr
PHASE ROTATOR
34
EQUALIZER
9
17-2
Ia
Qa
16-3
IDENTIFIER
10
Id
Qd
P/S CONVERTER
11
EQUALIZER
19
16-2
16-1
MEMORY
13
Ir'
Qr'
14
EQUALIZER
TAP COEFFICIENT UPDATING UNIT
15
17-1
17-3
Ia'
Qa'
Iab'
Qab'
Ei
Eq
20
EQUALIZER
TAP COEFFICIENT UPDATING UNIT
21
TRAINING SIGNAL GENERATOR
18
It
Qt
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
12

FIG.14

FIG.15

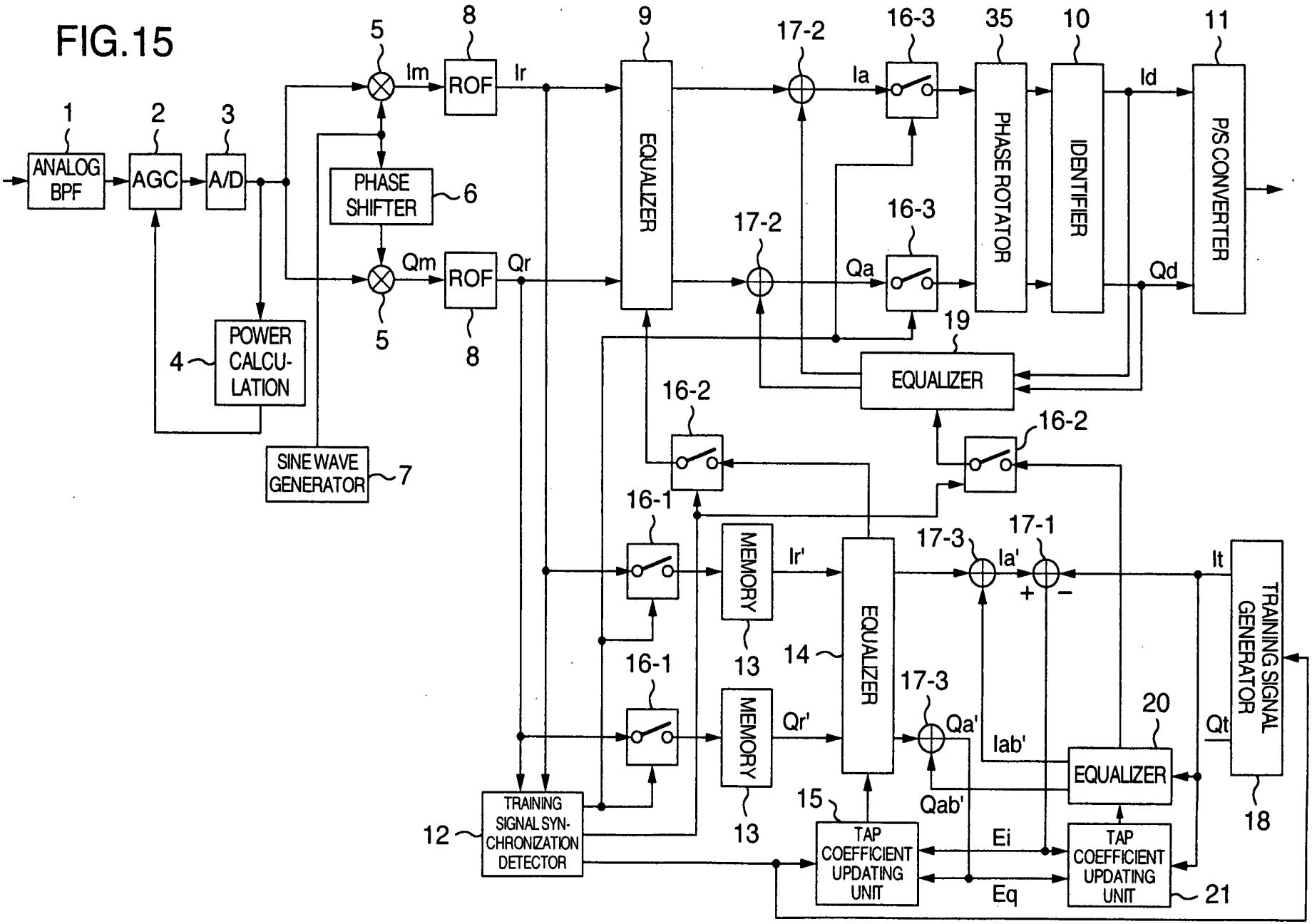
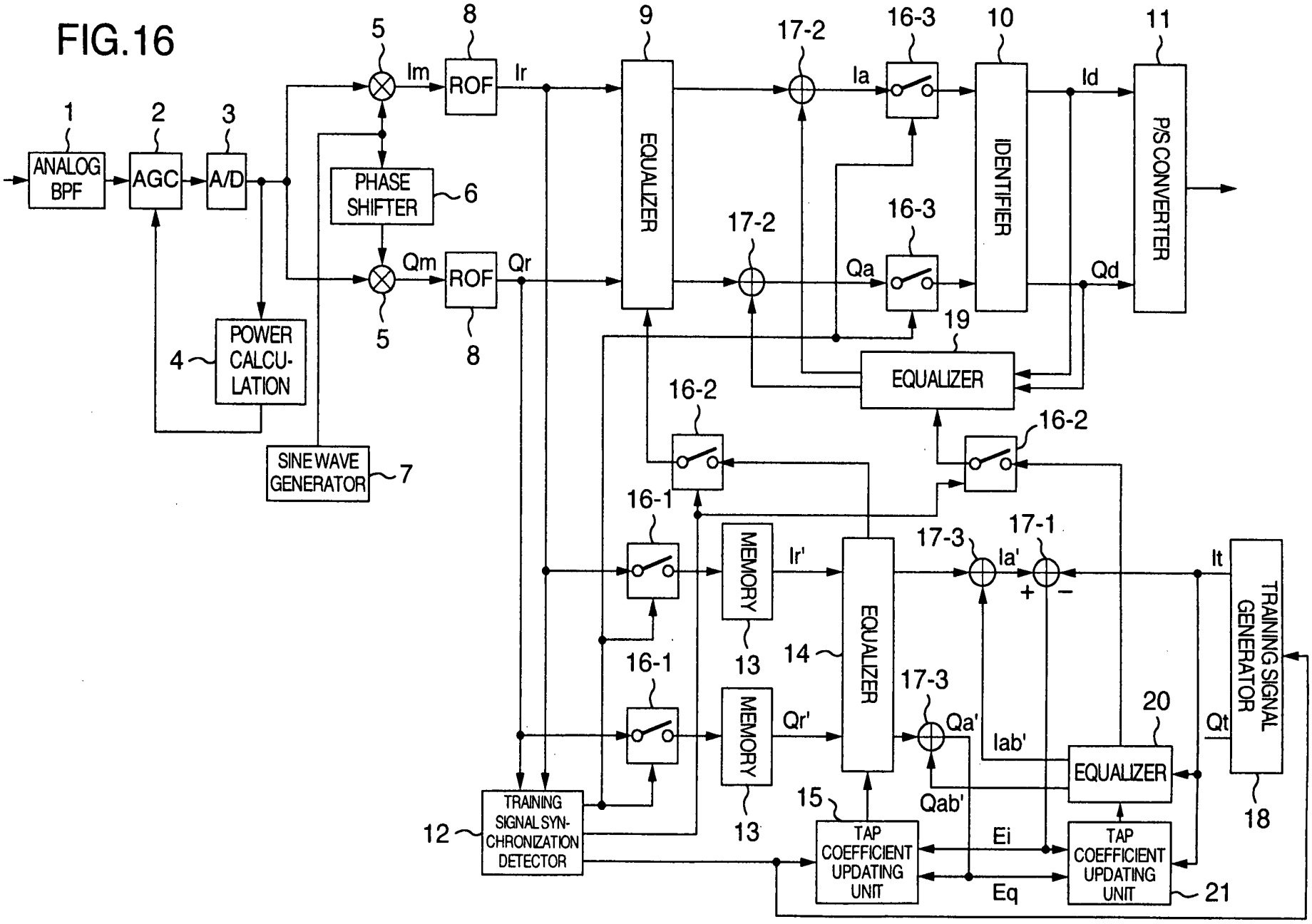

1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCU-LATION
5
Im
5
Qm
6
PHASE SHIFTER
7
SINE WAVE GENERATOR
8
ROF
Ir
8
ROF
Qr
9
EQUALIZER
17-2
17-2
16-3
Ia
16-3
Qa
35
PHASE ROTATOR
10
IDENTIFIER
11
P/S CONVERTER
Id
Qd
19
EQUALIZER
16-2
16-2
16-1
16-1
MEMORY
Ir'
13
MEMORY
Qr'
13
14
EQUALIZER
17-3
Ia'
17-1
+
−
It
17-3
Qa'
Iab'
Qab'
20
EQUALIZER
Qt
TRAINING SIGNAL GENERATOR
18
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
TAP COEFFICIENT UPDATING UNIT
21

FIG.16


1
ANALOG BPF
2
AGC
3
A/D
4
POWER CALCU-LATION
5
Im
ROF
8
Ir
PHASE SHIFTER
6
Qm
ROF
Qr
5
8
SINE WAVE GENERATOR
7
9
EQUALIZER
17-2
16-3
Ia
10
IDENTIFIER
Id
11
P/S CONVERTER
17-2
16-3
Qa
Qd
19
EQUALIZER
16-2
16-2
16-1
16-1
MEMORY
Ir'
13
14
EQUALIZER
17-3
Ia'
17-1
+
−
It
TRAINING SIGNAL GENERATOR
18
MEMORY
Qr'
13
17-3
Qa'
Iab'
20
EQUALIZER
Qt
Qab'
12
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
15
TAP COEFFICIENT UPDATING UNIT
Ei
Eq
TAP COEFFICIENT UPDATING UNIT
21

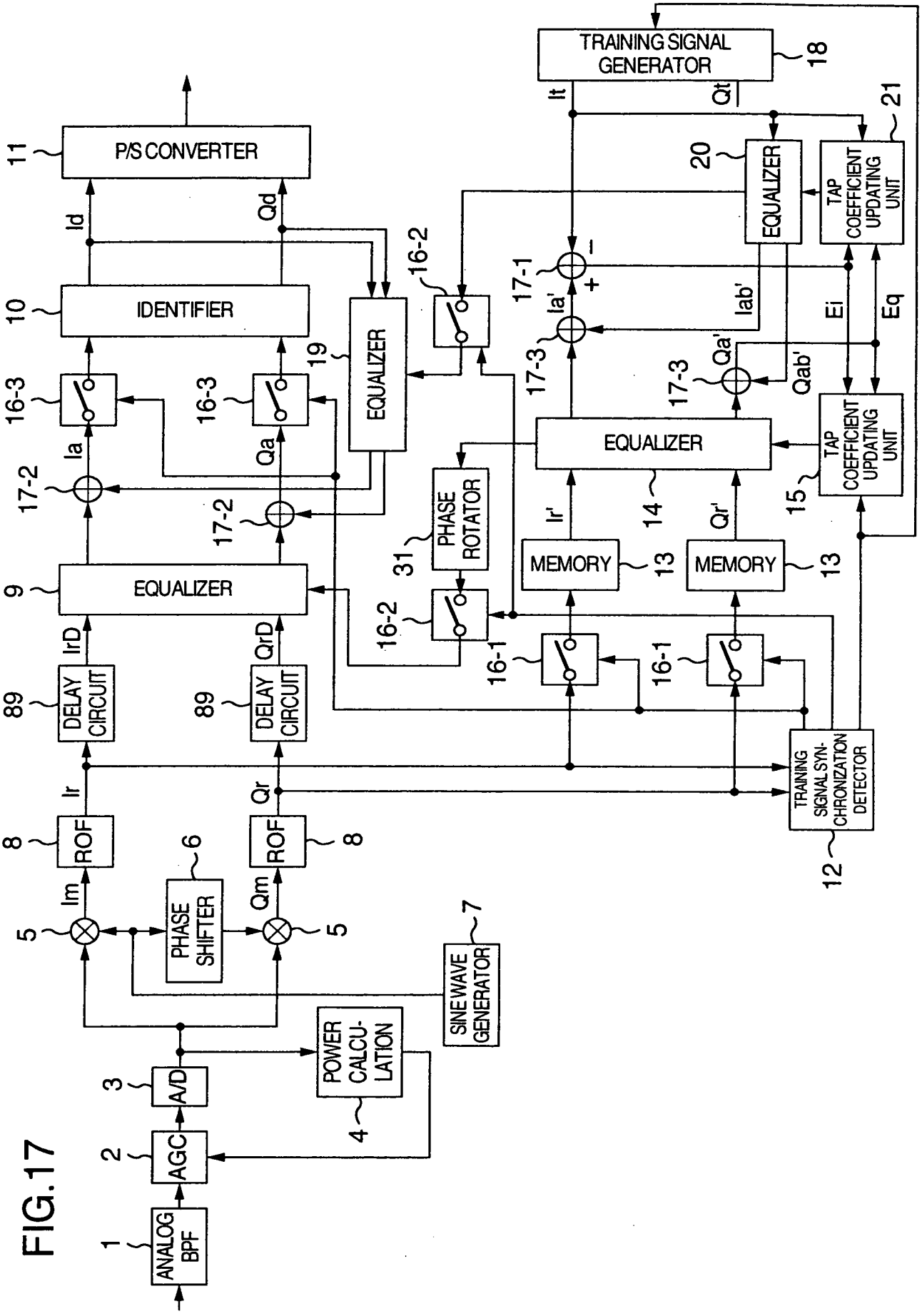

ANALOG BPF
1
AGC
2
A/D
3
POWER CALCU-LATION
4
SINEWAVE GENERATOR
7
PHASE SHIFTER
6
5
Im
Qm
ROF
8
Ir
Qr
DELAY CIRCUIT
89
IrD
QrD
EQUALIZER
9
IDENTIFIER
10
P/S CONVERTER
11
Id
Qd
16-3
Ia
Qa
17-2
19
16-2
31
PHASE ROTATOR
16-1
MEMORY
13
Ir'
Qr'
14
EQUALIZER
TAP COEFFICIENT UPDATING UNIT
15
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
12
TRAINING SIGNAL GENERATOR
18
It
Qt
20
21
17-1
17-3
Ia'
Iab'
Qa'
Qab'
Ei
Eq

FIG.17

FIG.18

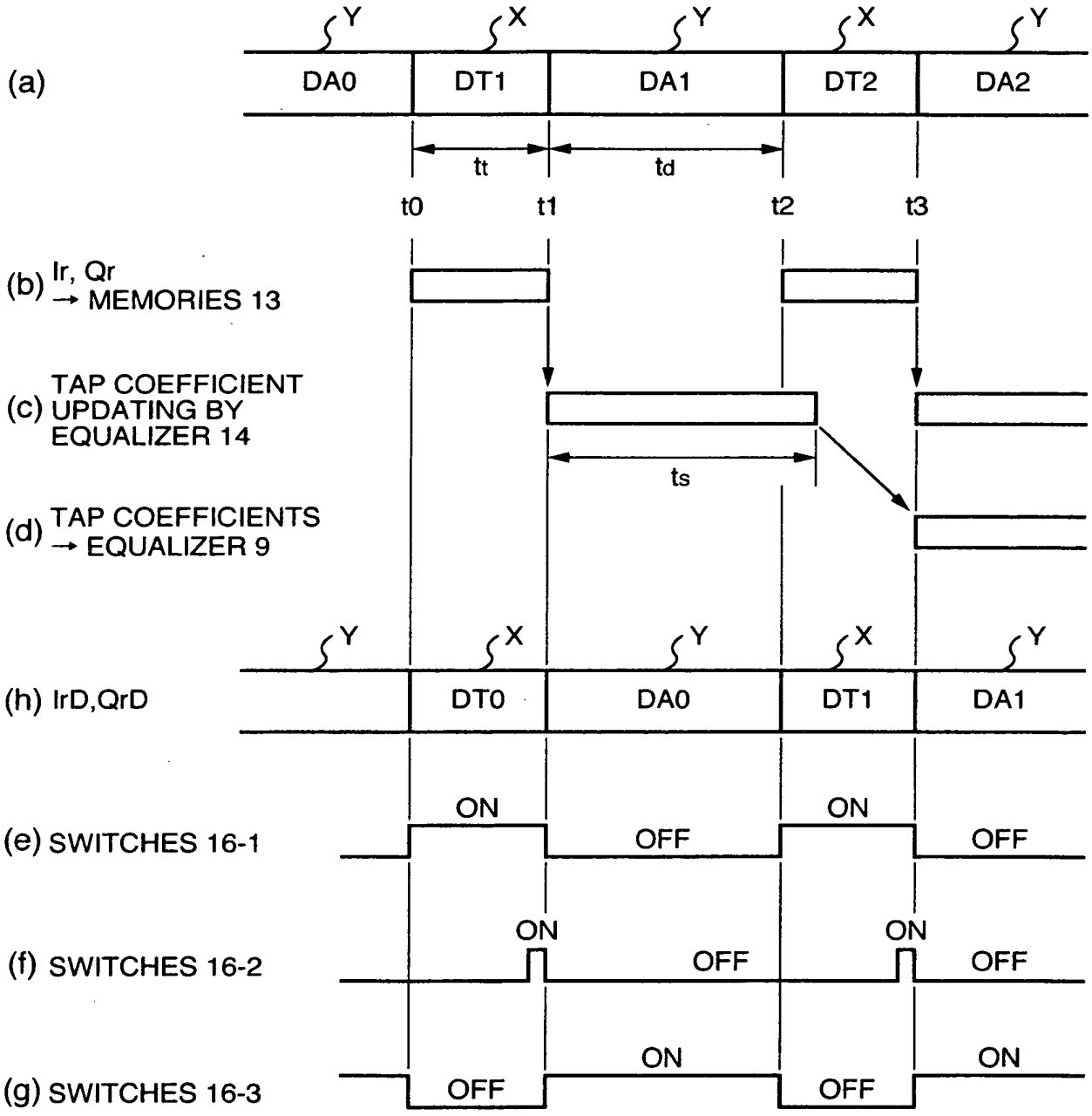

(a)
Y
X
Y
X
Y
DA0
DT1
DA1
DT2
DA2
tt
td
t0
t1
t2
t3
(b) Ir, Qr → MEMORIES 13
(c) TAP COEFFICIENT UPDATING BY EQUALIZER 14
ts
(d) TAP COEFFICIENTS → EQUALIZER 9
(h) IrD,QrD
DT0
DA0
DT1
DA1
(e) SWITCHES 16-1
ON
OFF
(f) SWITCHES 16-2
(g) SWITCHES 16-3

FIG.19

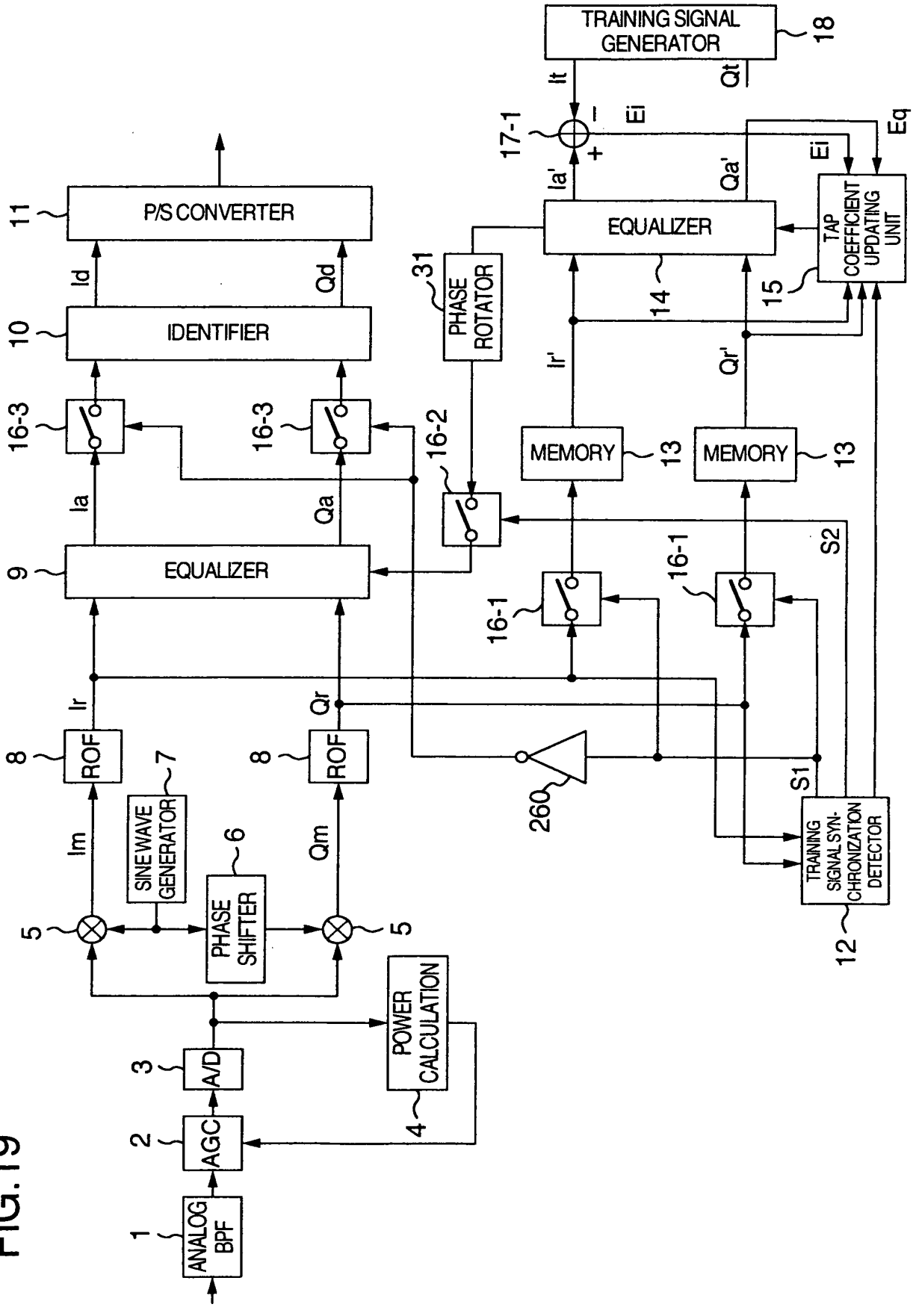

TRAINING SIGNAL GENERATOR
18
It
Qt
17-1
Ei
Eq
Ei
Ia'
Qa'
EQUALIZER
TAP COEFFICIENT UPDATING UNIT
14
15
31
PHASE ROTATOR
Ir'
Qr'
MEMORY
13
MEMORY
13
16-2
16-1
16-1
S2
S1
260
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
12
11
P/S CONVERTER
Id
Qd
10
IDENTIFIER
16-3
16-3
Ia
Qa
9
EQUALIZER
Ir
Qr
8
ROF
8
ROF
7
SINEWAVE GENERATOR
6
PHASE SHIFTER
Im
Qm
5
5
POWER CALCULATION
4
3
A/D
2
AGC
1
ANALOG BPF

FIG.20

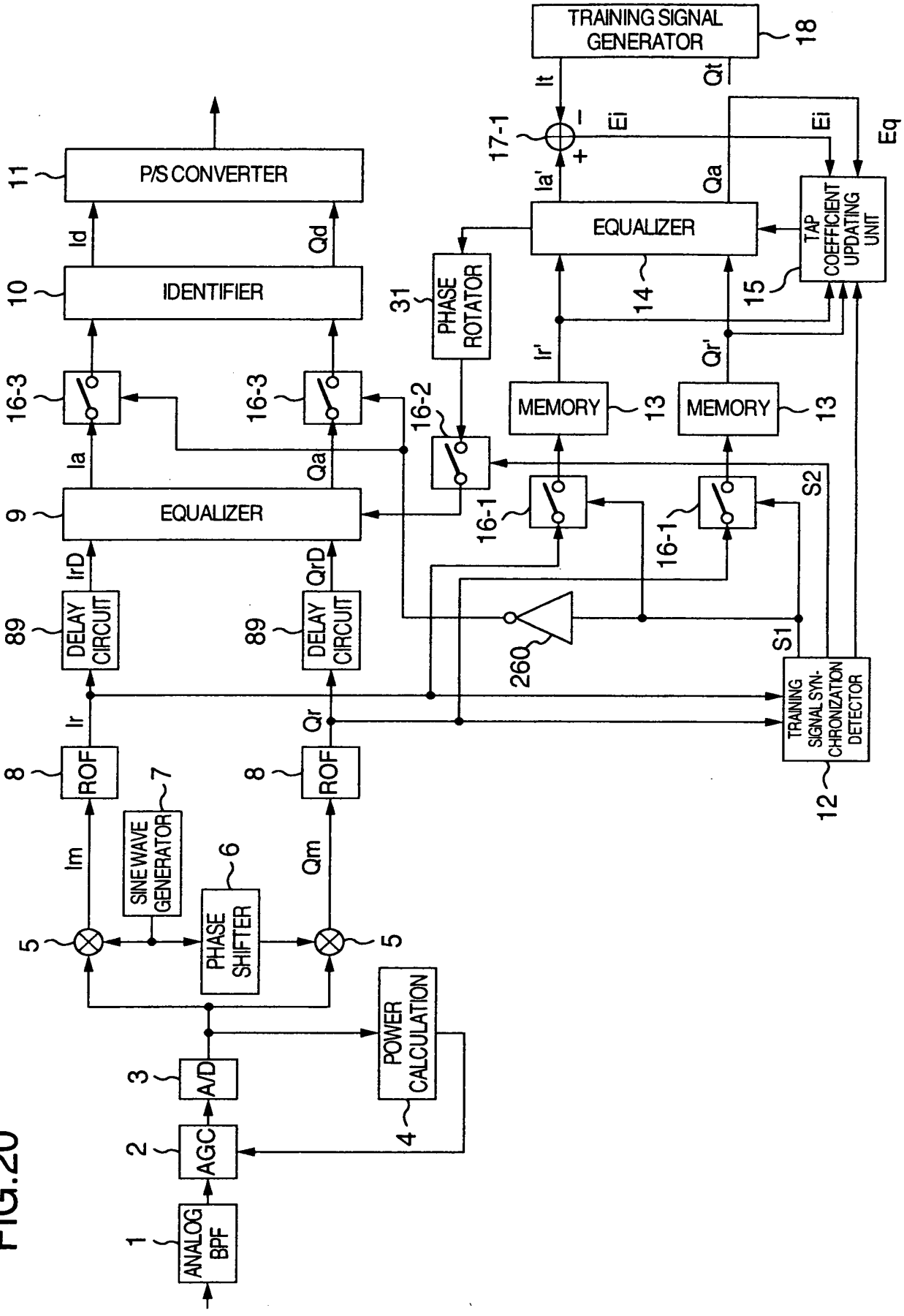
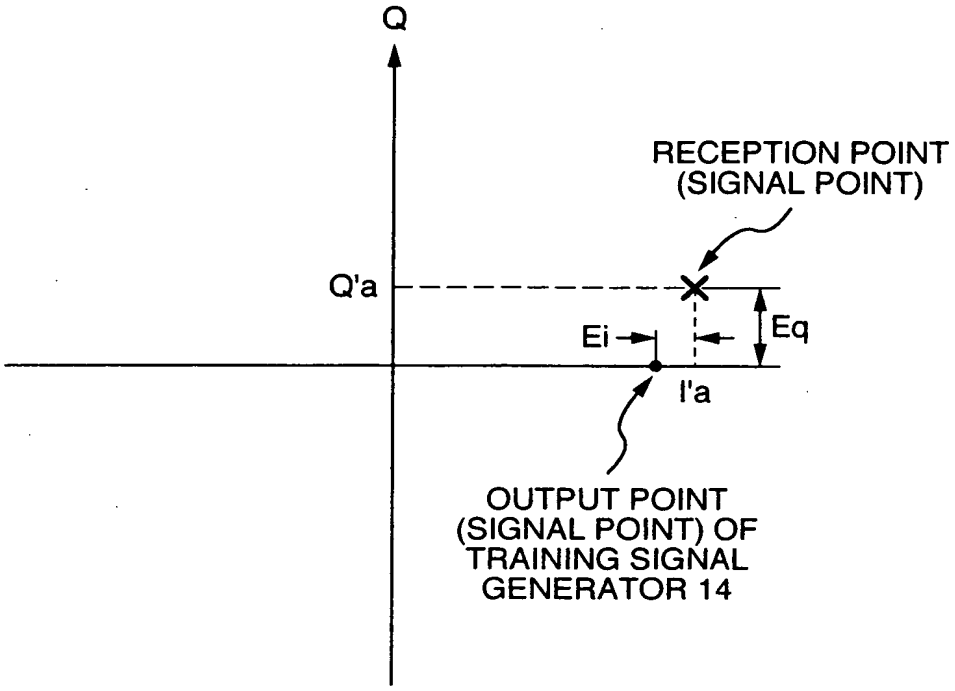

ANALOG BPF
1
AGC
2
A/D
3
POWER CALCULATION
4
5
SINE WAVE GENERATOR
7
PHASE SHIFTER
6
ROF
8
DELAY CIRCUIT
89
EQUALIZER
9
IDENTIFIER
10
P/S CONVERTER
11
TRAINING SIGNAL SYN-CHRONIZATION DETECTOR
12
MEMORY
13
EQUALIZER
14
TAP COEFFICIENT UPDATING UNIT
15
16-1
16-2
16-3
PHASE ROTATOR
31
TRAINING SIGNAL GENERATOR
18
17-1
260
S1
S2
Ir
Qr
Im
Qm
IrD
QrD
Id
Qd
Ia
Qa
Ir'
Qr'
Ia'
It
Qt
Ei
Eq

FIG.21


Q
RECEPTION POINT
(SIGNAL POINT)
Q'a
Ei
Eq
I'a
OUTPUT POINT
(SIGNAL POINT) OF
TRAINING SIGNAL
GENERATOR 14